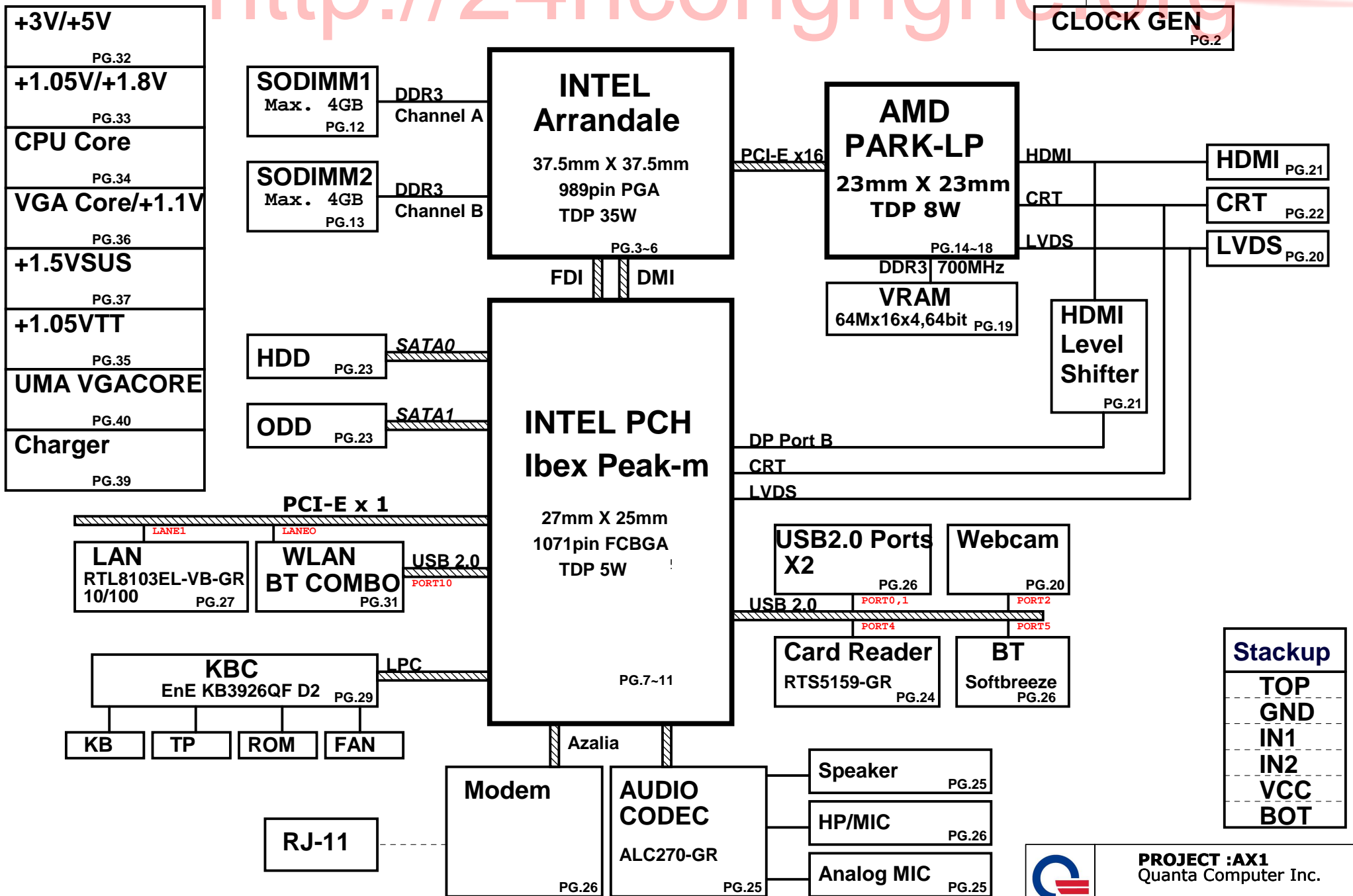
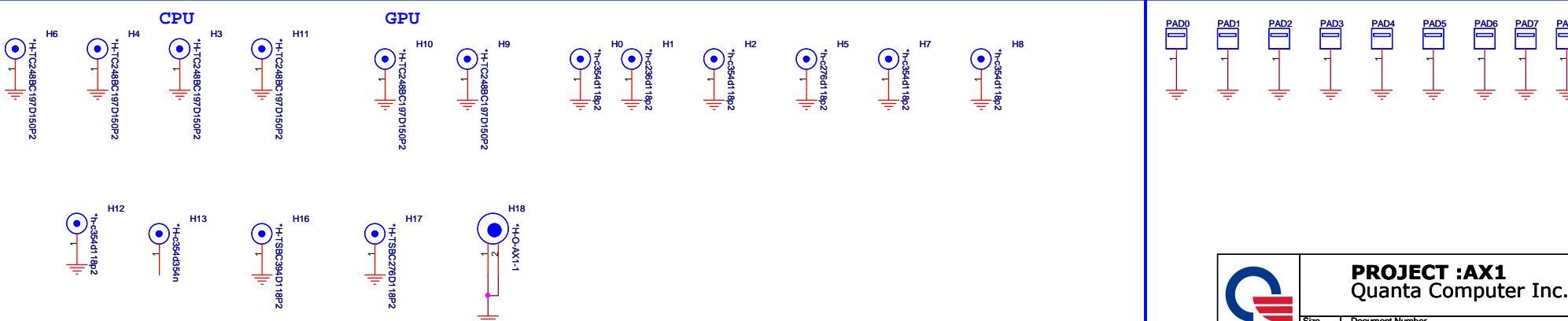
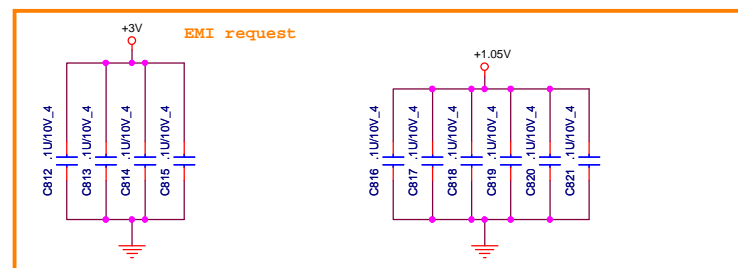
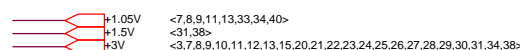
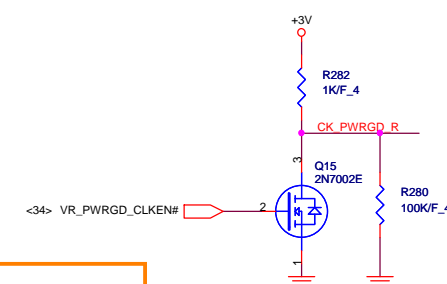
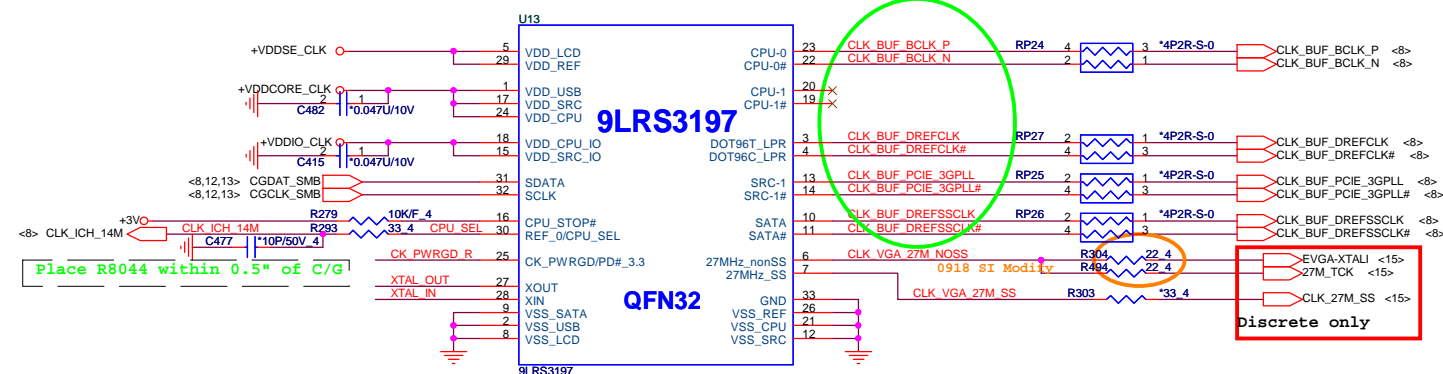
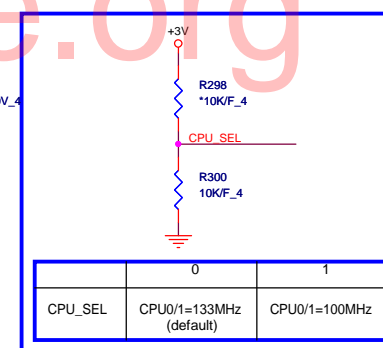
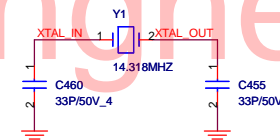
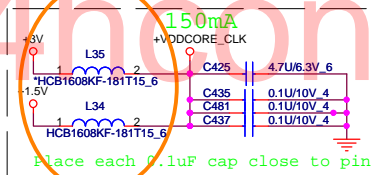
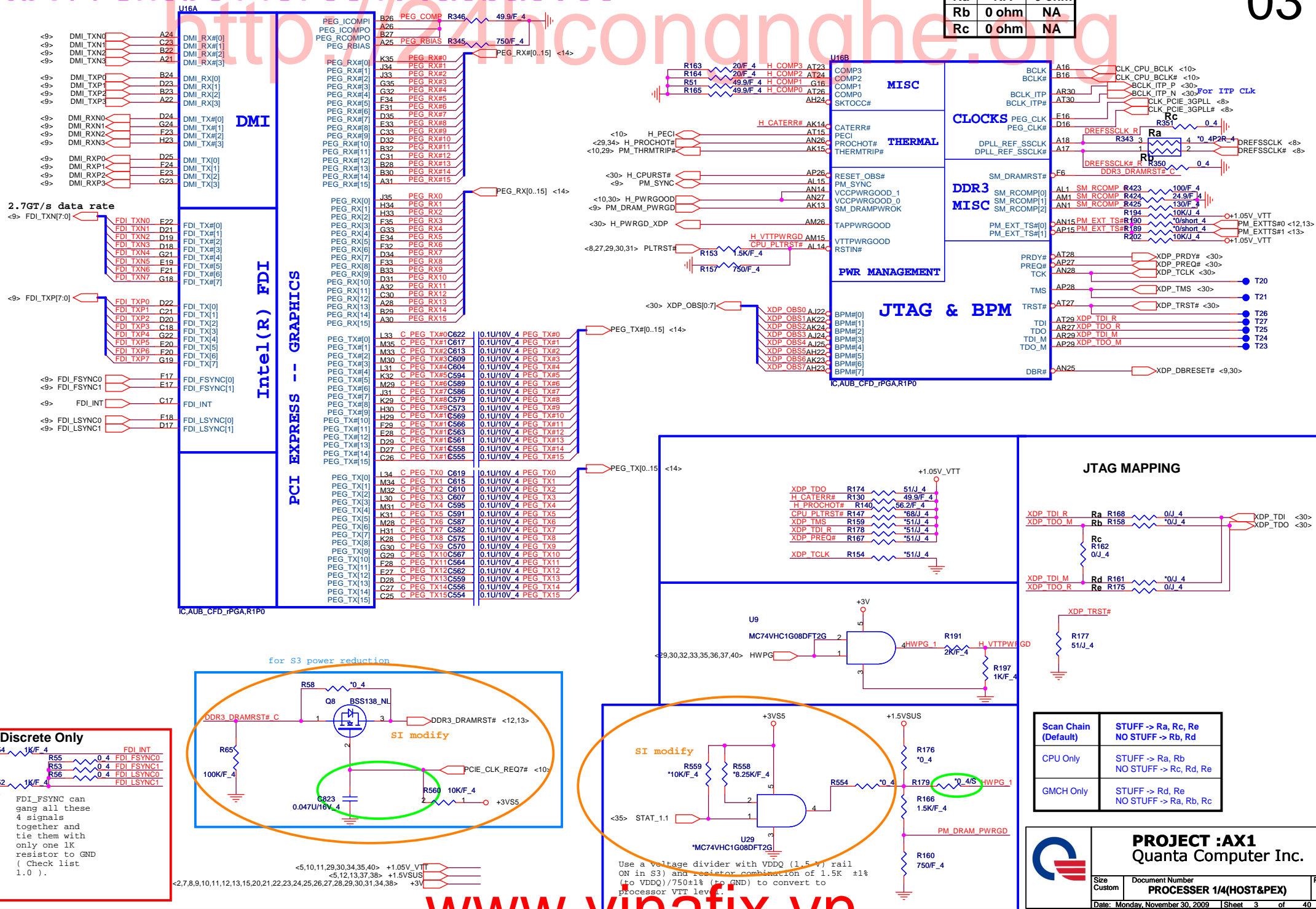


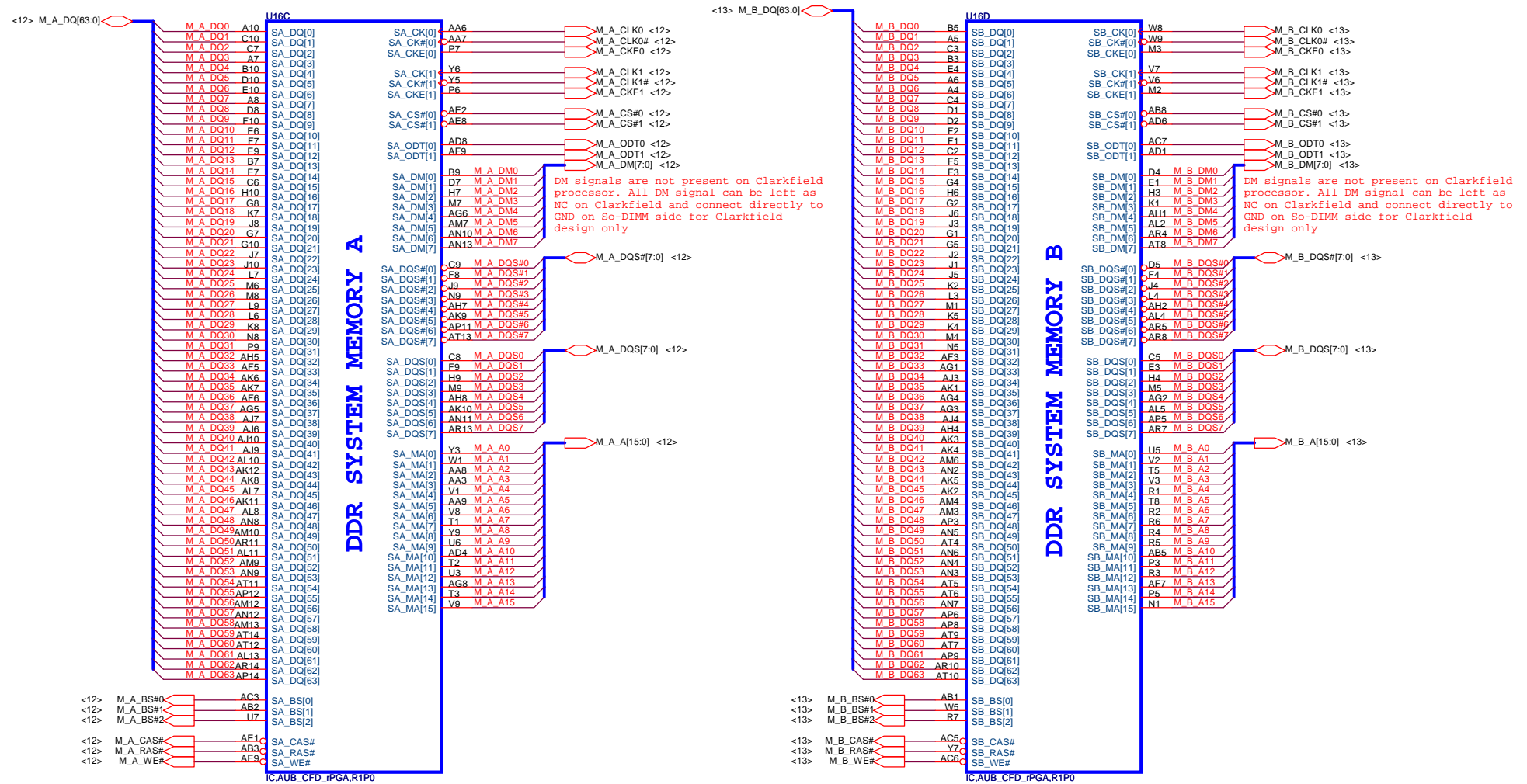
AX1 INTEL UMA/DISCRETE SYSTEM DIAGRAM





	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

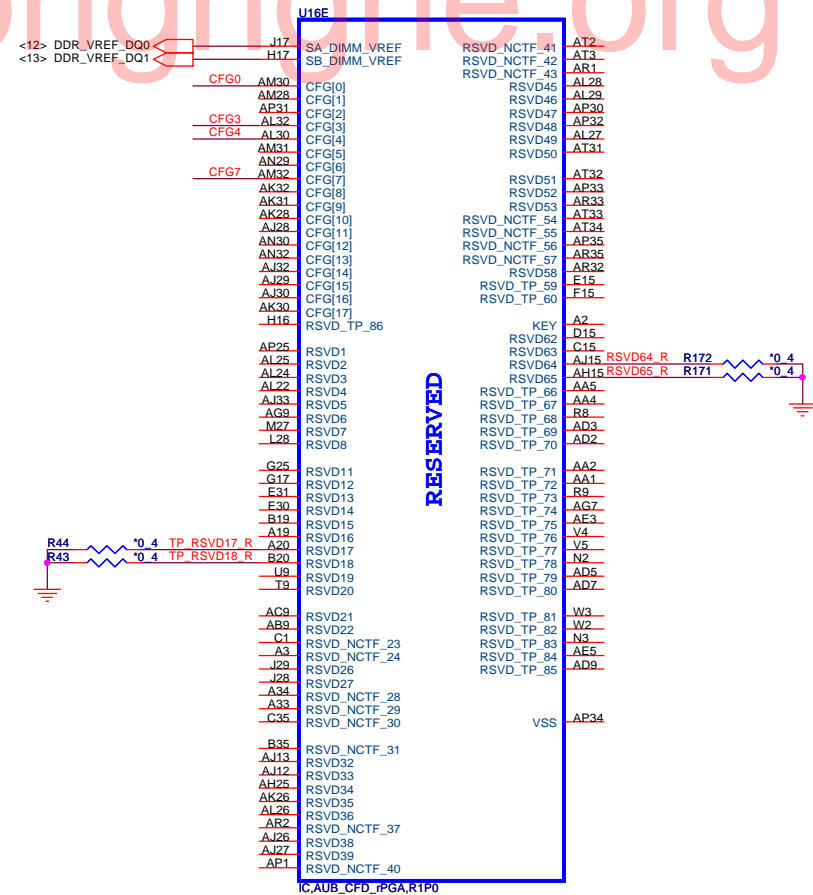
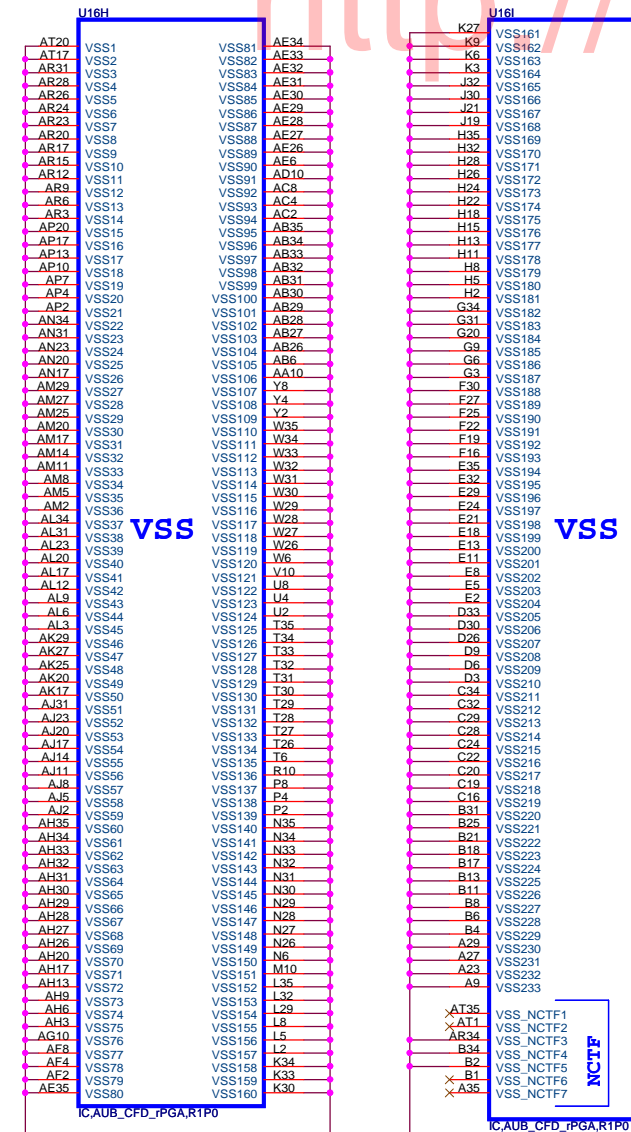






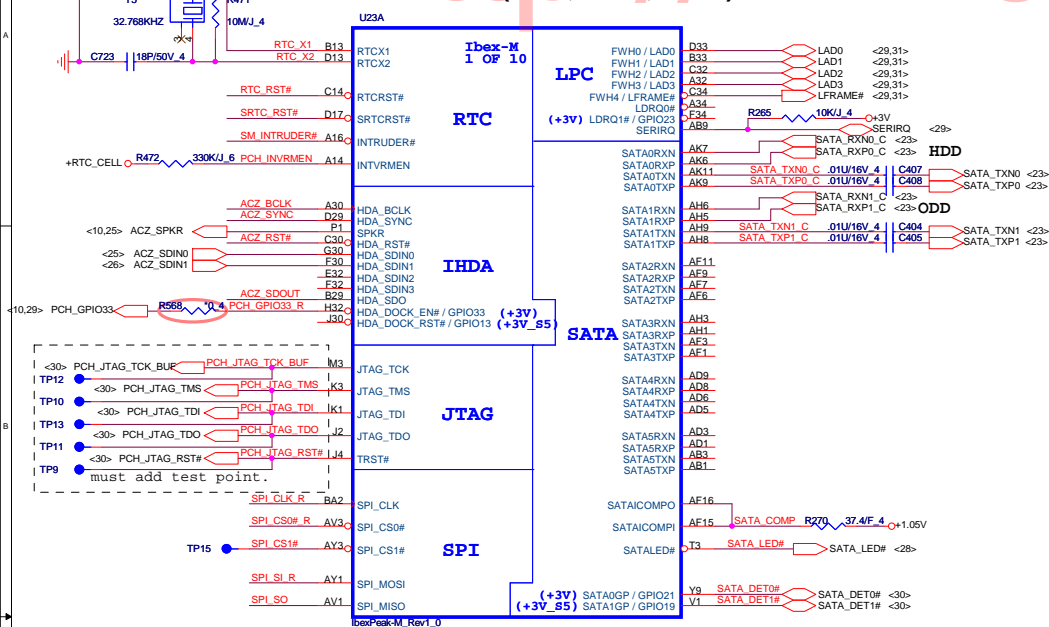
AUBURNDAL/CLARKSFIELD PROCESSOR (GND)

AUBURNDAL/CLARKSFIELD PROCESSOR (RESERVED, CFG)



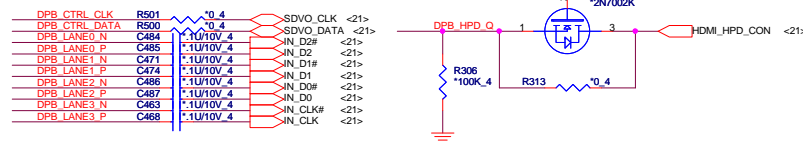
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

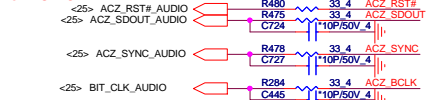


1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

UMA HDMI signals



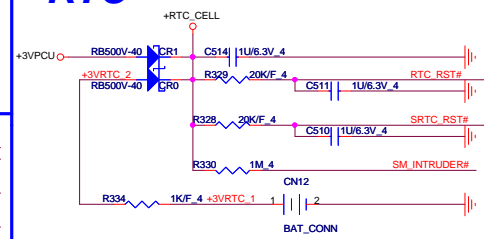
For AUDIO



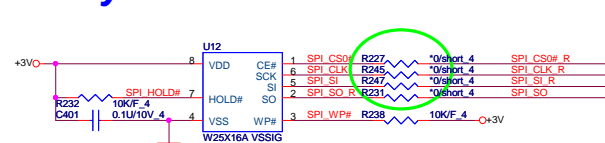
For MDC



RTC

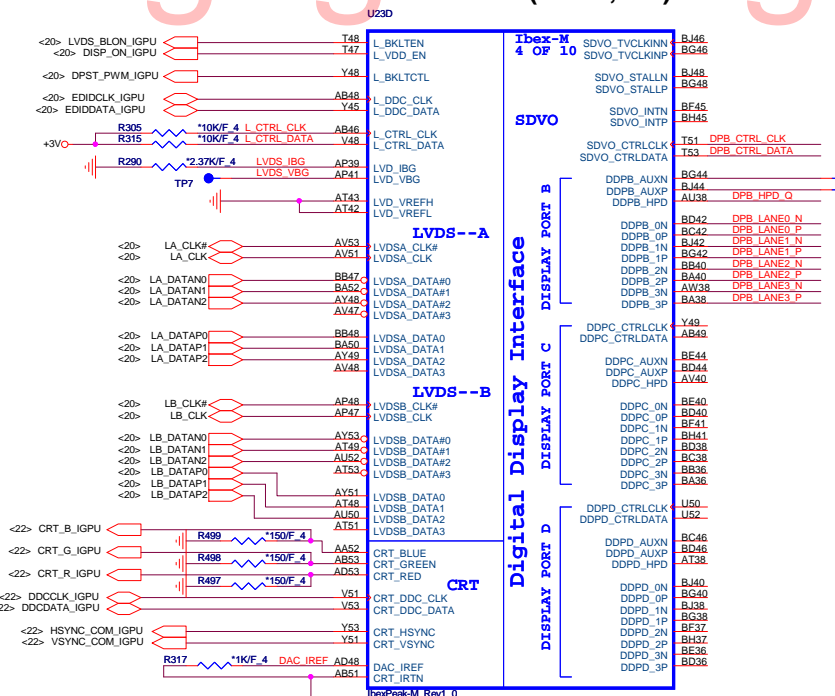


4M byte SPI ROM



UMA CRT,LVDS&HDMI signals

IBEX PEAK-M (LVDS,DDI)



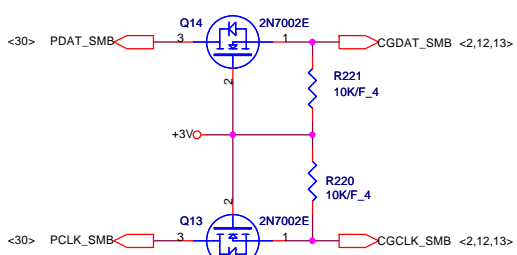
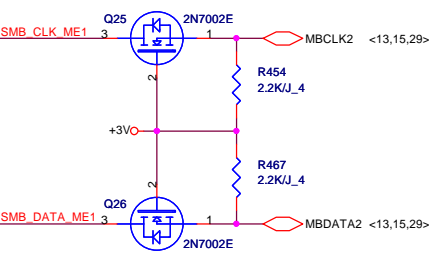
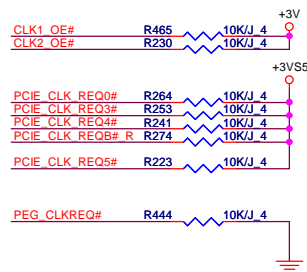
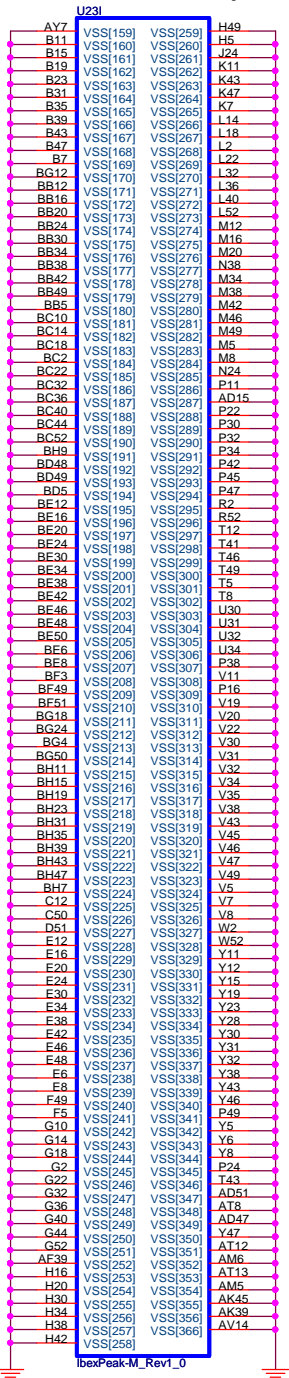
Vendor	PN
Socket	DG008000031
WINBOND	AKE39ZPN00
MAX	AKE39FPN00



PROJECT :AX1
Quanta Computer Inc.

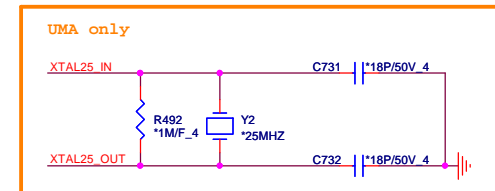
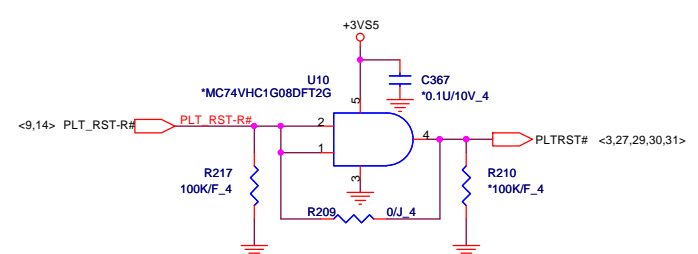
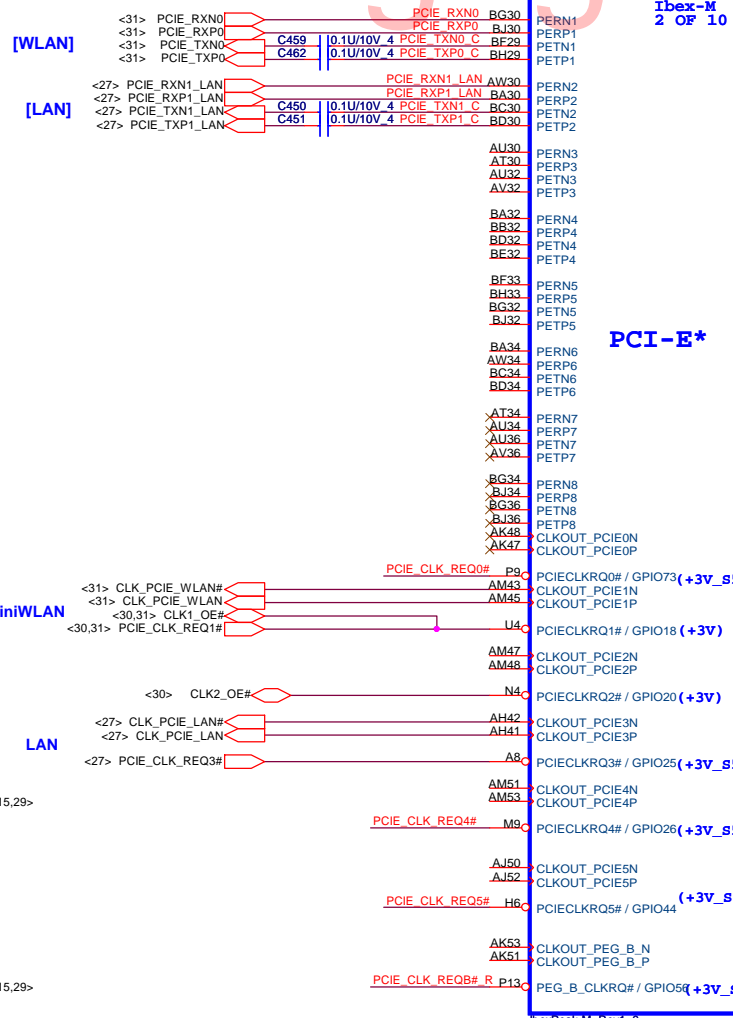
Size	Document Number	Rev
Custom	PCH 1/5 (SATA,HDA,LPC)	1A
Date: Monday, November 30, 2009	Sheet 7 of 40	

IBEX PEAK-M (GND)



IBEX PEAK-M (PCI-E,SMBUS,CLK)

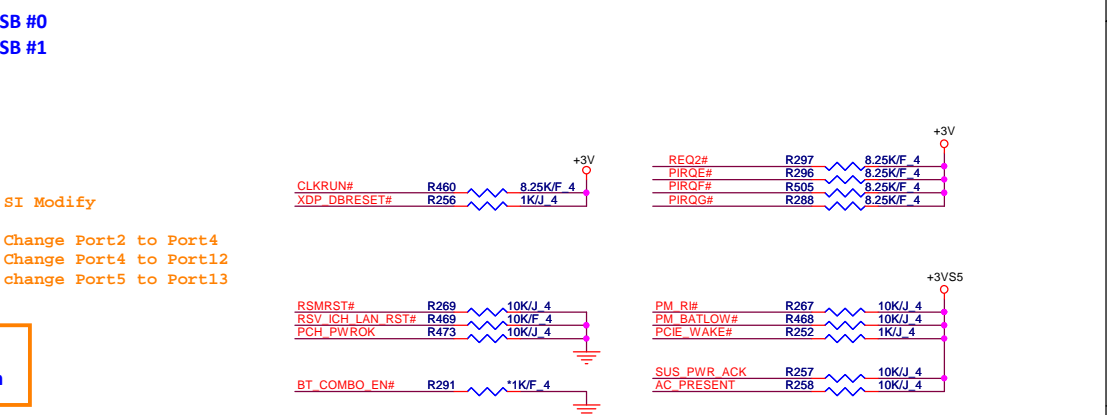
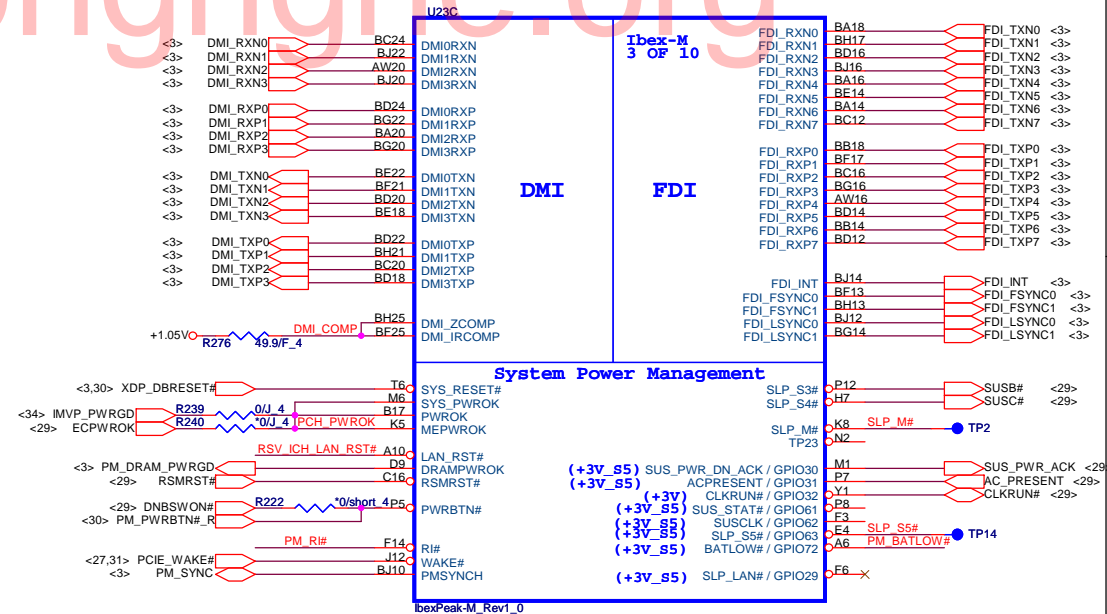
U23B



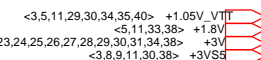
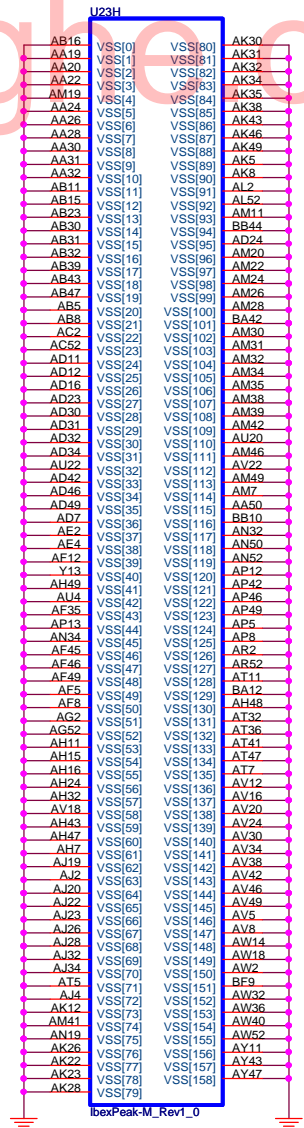
PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/5 (PCIE, SMBUS, CK)	1A
Date: Monday, November 30, 2009 Sheet 8 of 40		

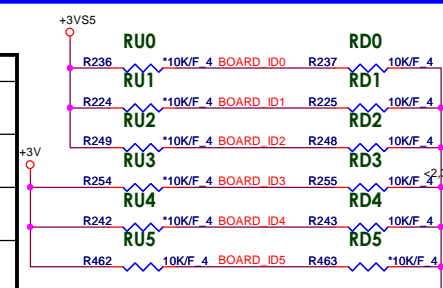
IBEX PEAK-M (DMI,FDI,GPIO)

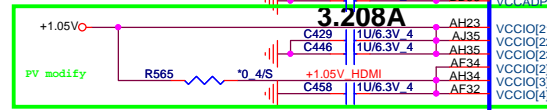
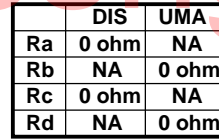


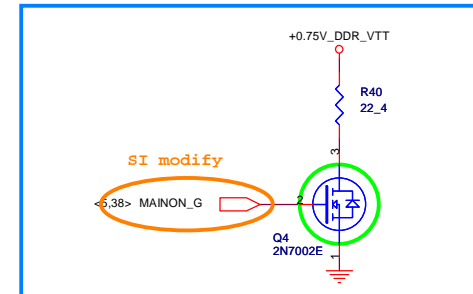
10



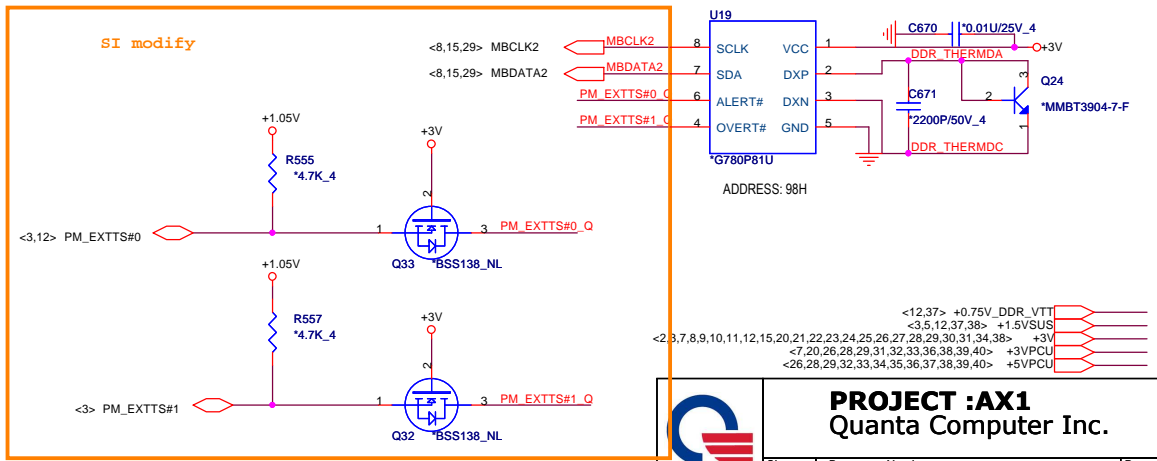
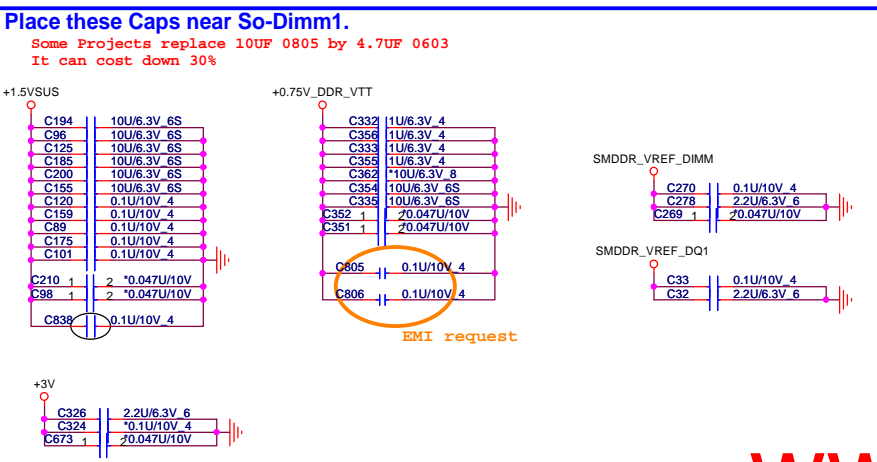
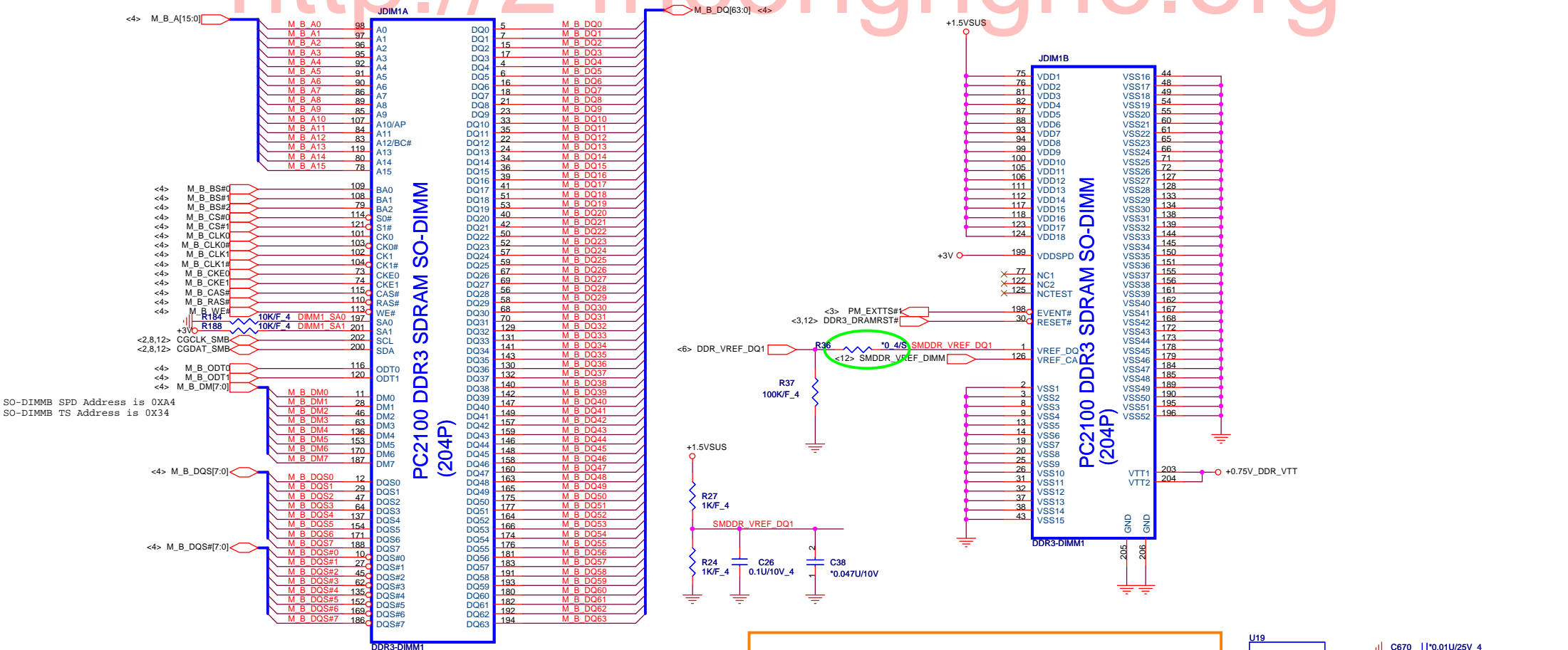
Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UMA FF	0	0	0	0	0	0
UMA DF	0	0	0	0	1	0
DIS	0	0	0	0	0	1





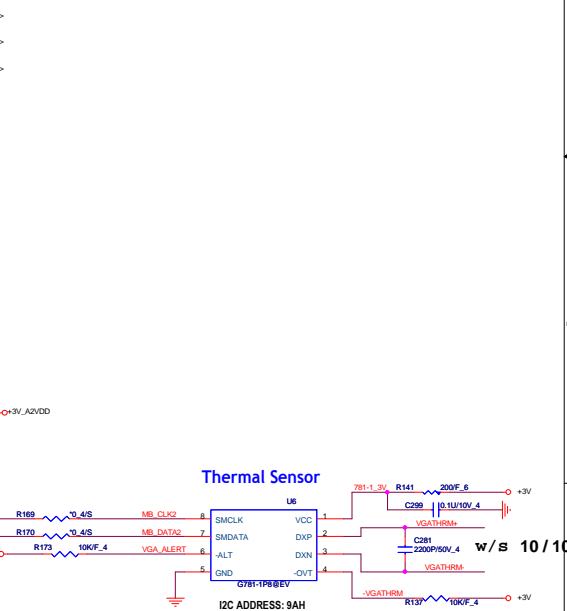
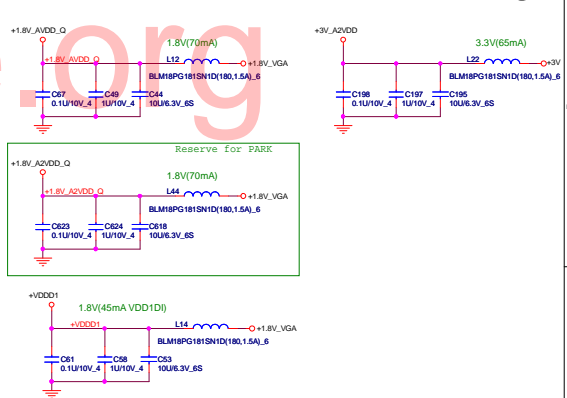



	<13,37>	+0.75V_DDR_VTT	
	<3,5,13,37,38>	+1.5VSUS	
<2,3,7,8,9,10,11,13,15,20,21,22,23,24,25,26,27,28,29,30,31,34,38>		+3V	
<7,20,26,28,29,31,32,33,36,38,39,40>		+3VPCU	
<26,28,29,32,33,34,35,36,37,38,39,40>		+5VPCU	

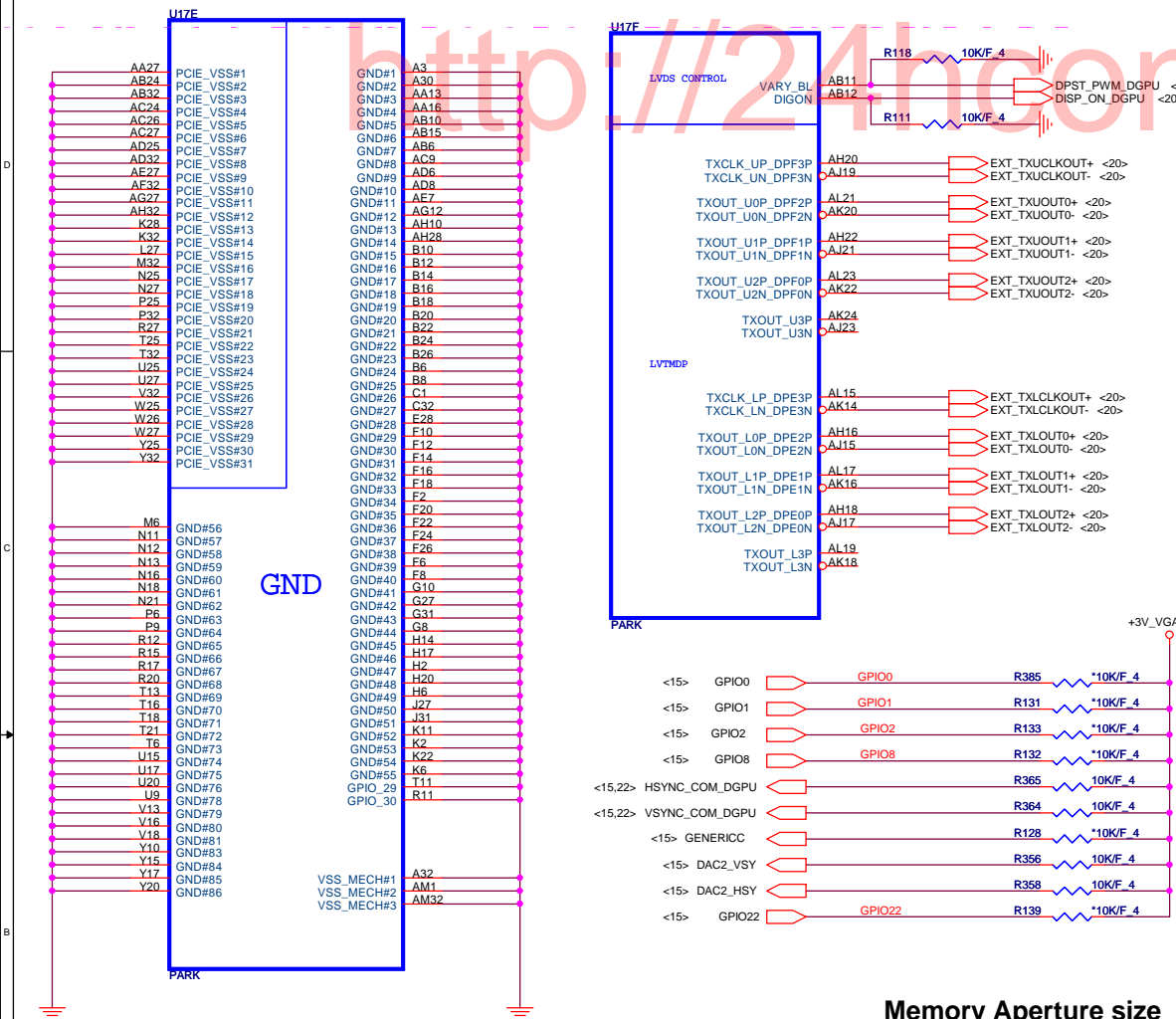




	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.95V
H	1	0	1.05V
TBD	1	1	NA



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	Size Custom Document Number M93_MAIN	Rev 1A
Date: Thursday, November 12, 2009 Sheet 15 of 40		



CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0 = DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET	
H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPIO21_BB_EN	

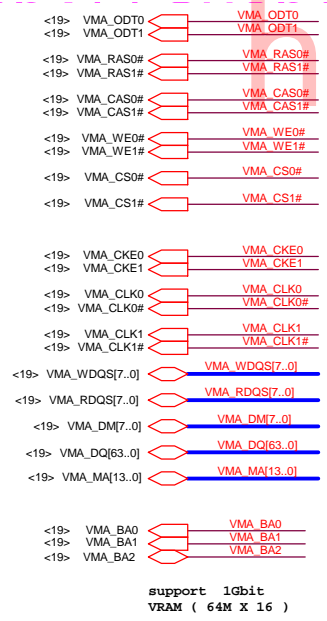
Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

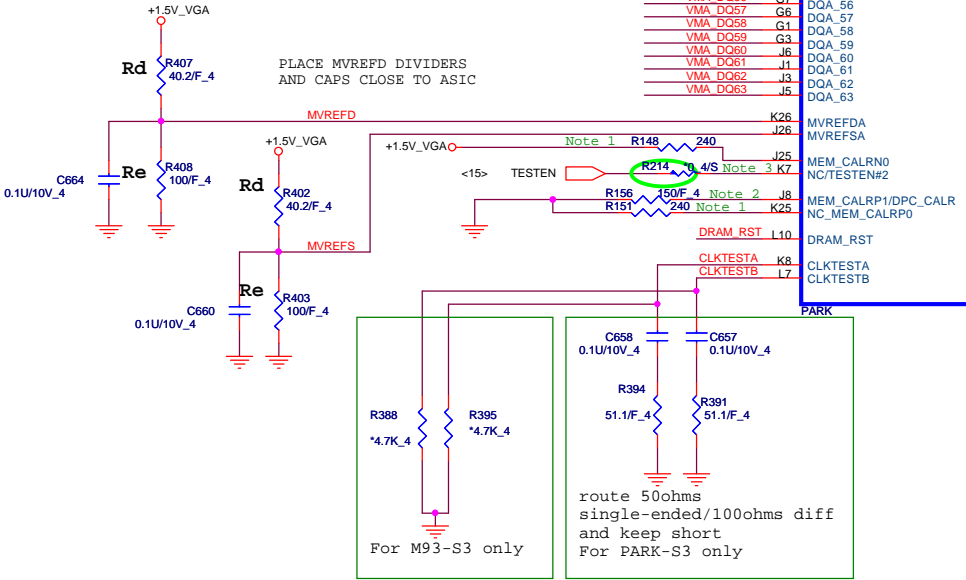
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



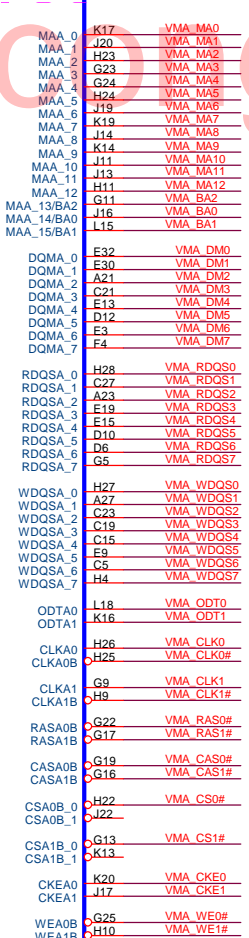
MEMORY INTERFACE



DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Rd)	40.2R	40.2R
MVREF TO GND (Re)	100R	100R



Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24



For PARK-S3 only
For M9X-S2/S3 with
DDR3: this pin is
not in use.

Designator	M9X-S2 and M93-S3	Park-S3
Ra	NC	10K
Rb	0R/Short	680R
Rc	2.2K	NC
Ca	2.2nF	68pF

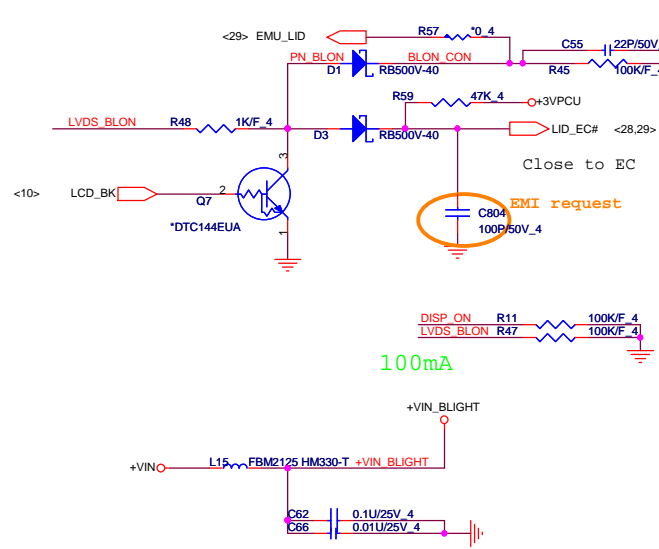


PROJECT :AX1
Quanta Computer Inc.

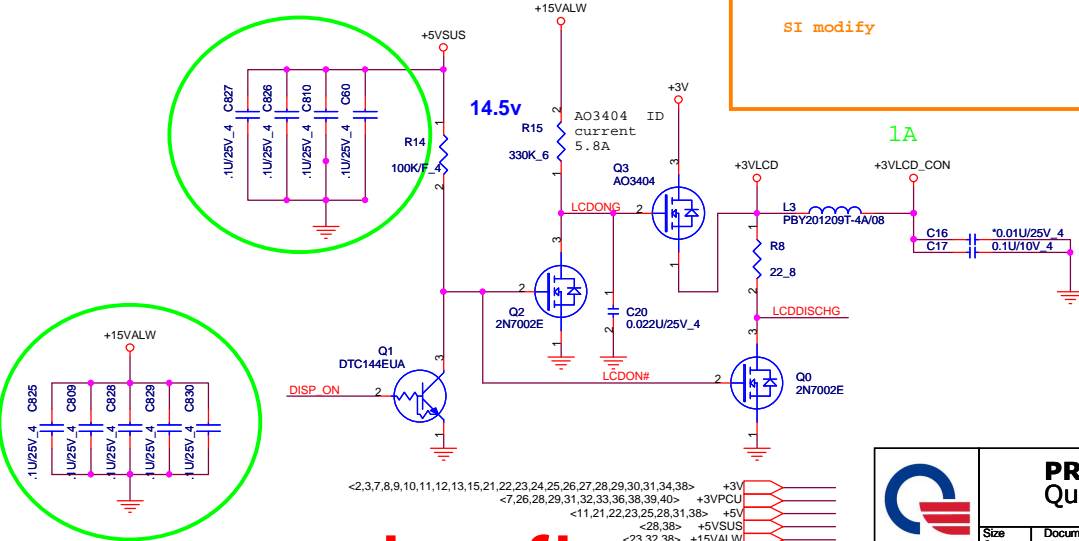
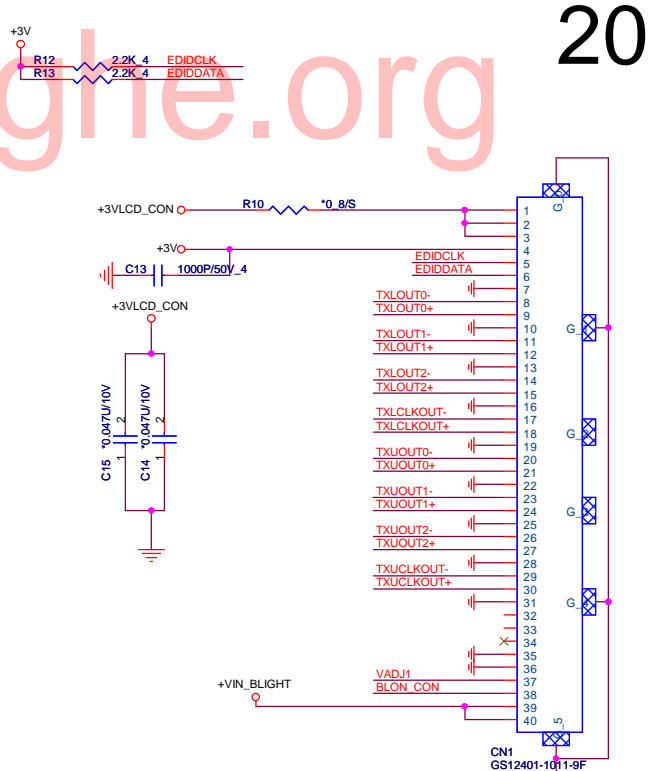
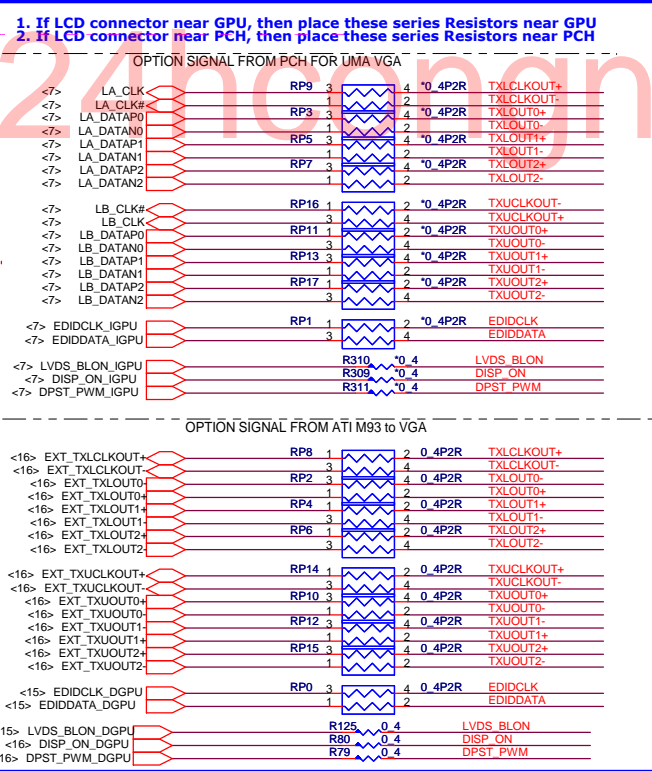
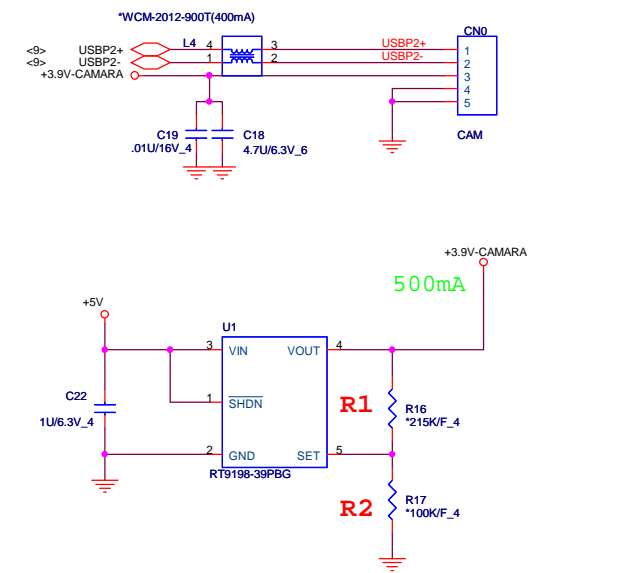
Size Custom	Document Number M93_MEM_Interface	Rev 1A
Date: Thursday, November 12, 2009		Sheet 18 of 40



LID Switch

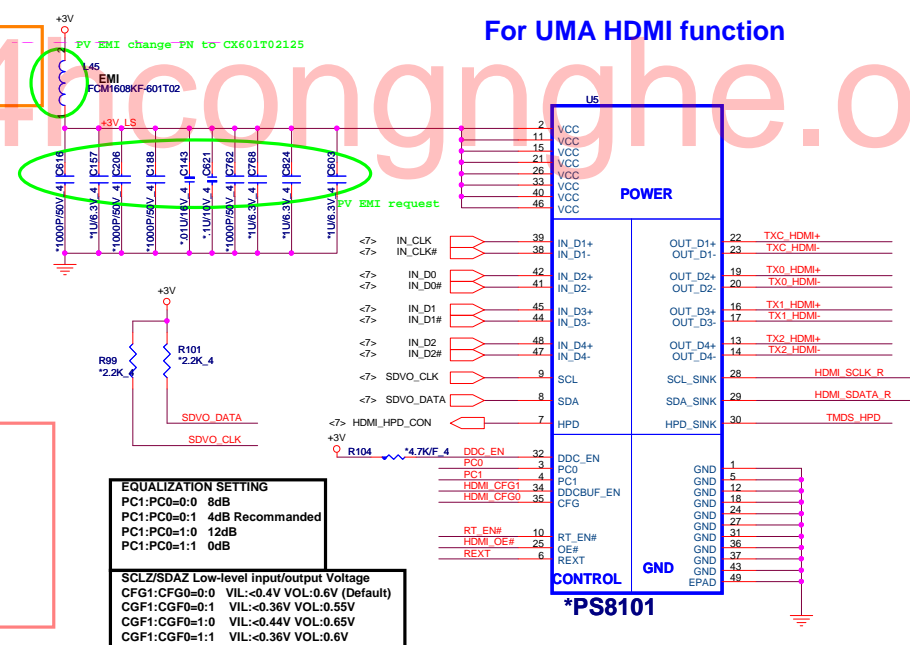
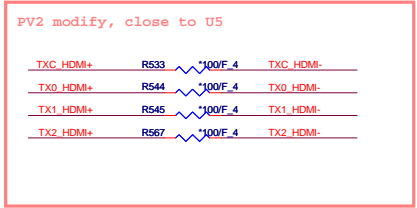


CAMERA

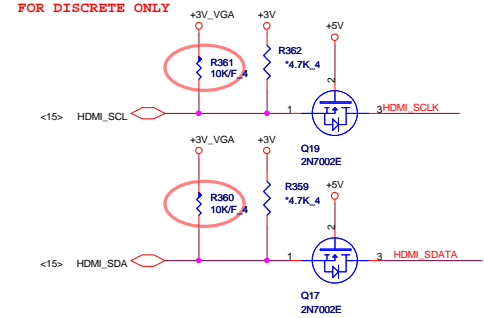


9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella
CHR : need Na R1182, add R1027 for capella

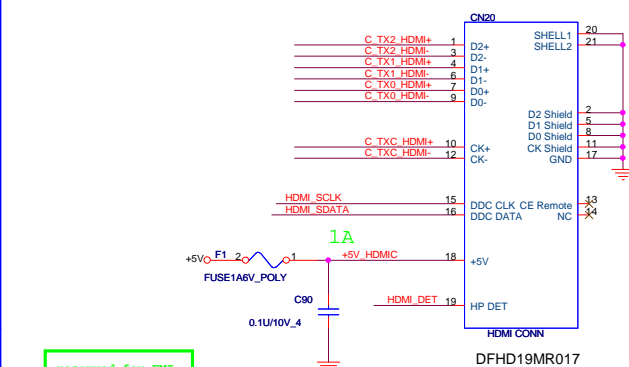
Vendor:PDT P/N:AL008101000
Vendor:CHR P/N:AL007318002
Vendor:PIM P/N:ALP411LS004



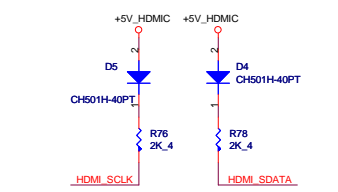
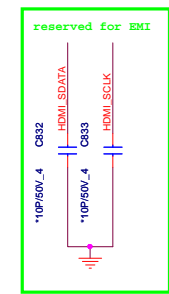
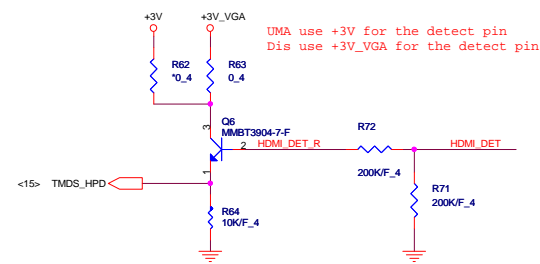
DISCRETE HDMI I2C SELECT
Close to HDMI Connector



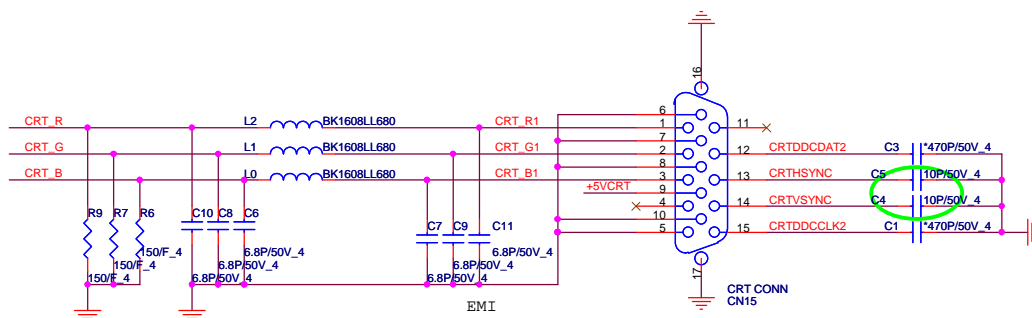
PV EMI request			
C TX2 HDMI+	R561	*100F/4	C TX2 HDMI-
C TX1 HDMI+	R562	*100F/4	C TX1 HDMI-
C TX0 HDMI+	R563	*100F/4	C TX0 HDMI-
C TXC HDMI+	R564	*100F/4	C TXC HDMI-



UMA & DISCRETEHDMI HPD SENSE

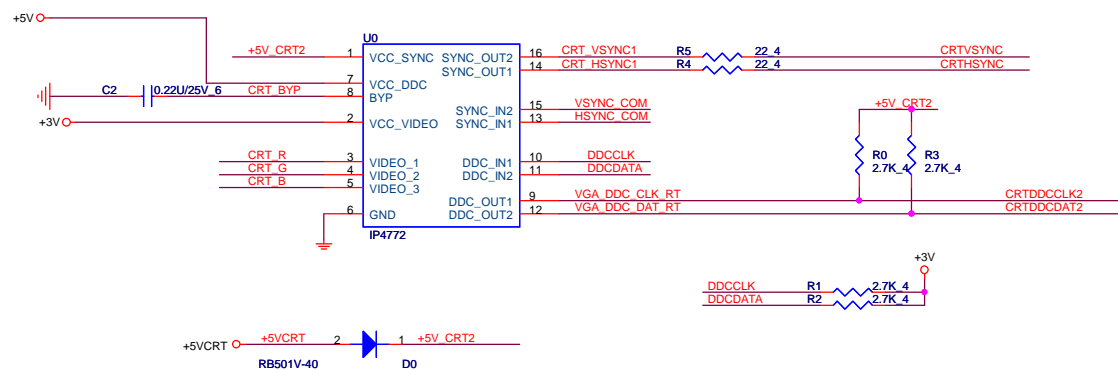


PORT <http://24hcongnghe.org>

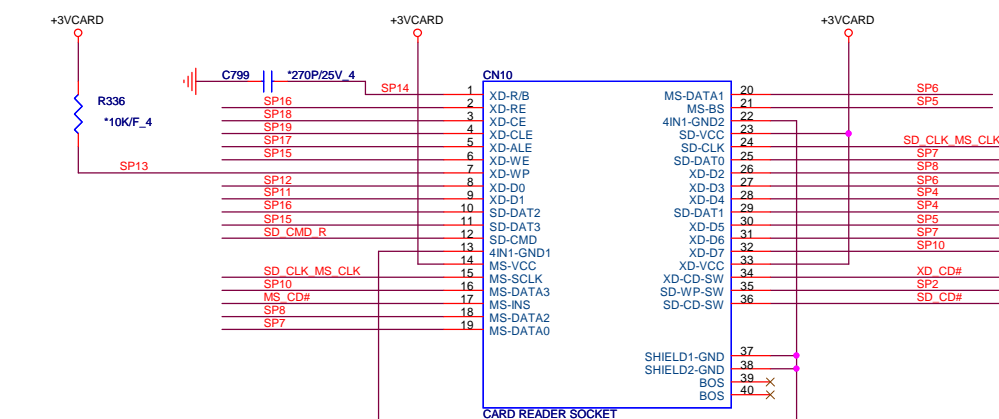
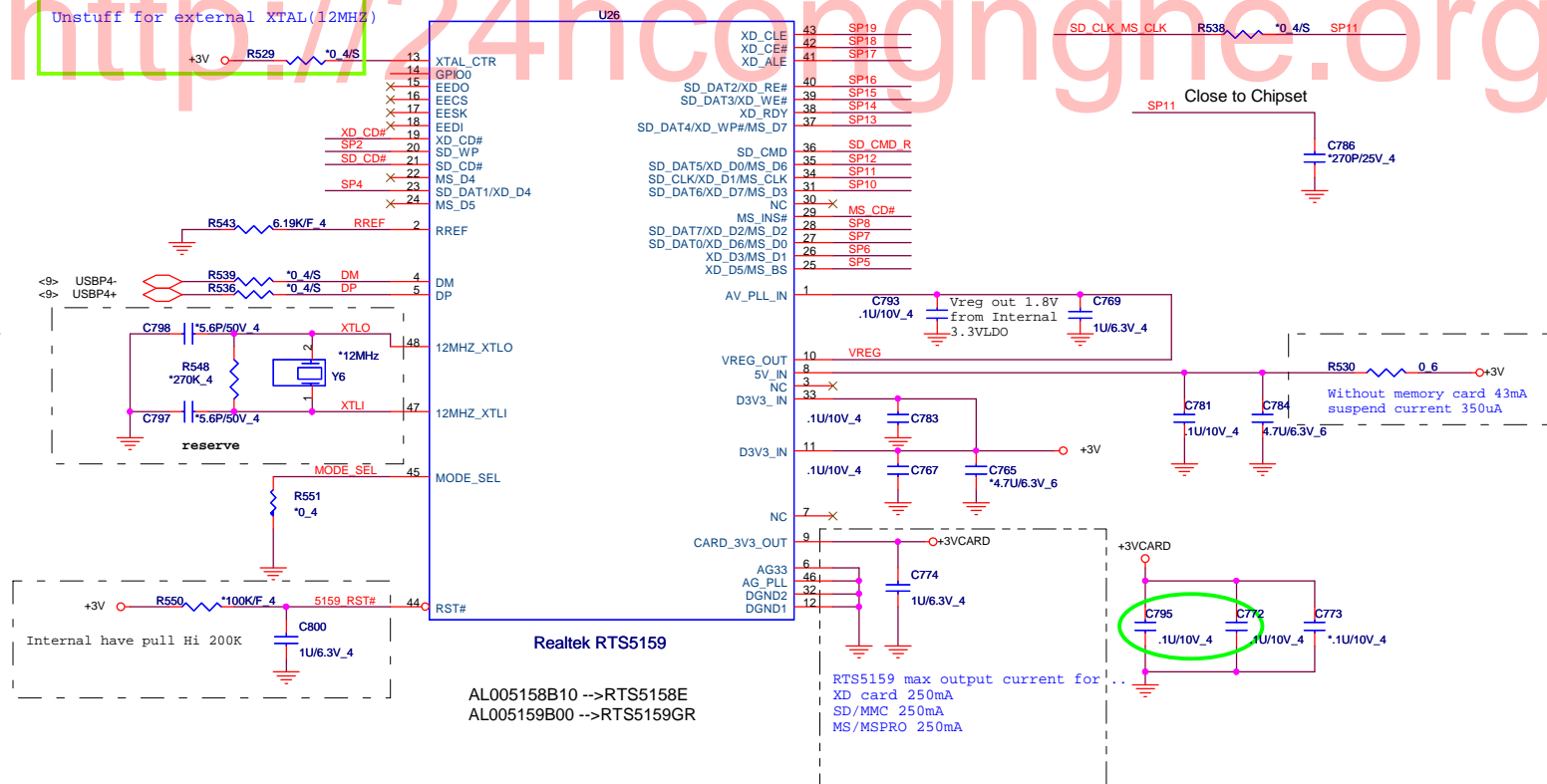


<7> CRT_R_IGPU	R23	0.4	CRT_R
<7> CRT_G_IGPU	R26	0.4	CRT_G
<7> CRT_B_IGPU	R29	0.4	CRT_B
<7> HSYNC_COM_IGPU	R21	0.4	HSYNC_COM
<7> VSYNC_COM_IGPU	R19	0.4	VSYNC_COM
<7> DDCCLK_IGPU	R32	0.4	DDCCLK
<7> DDCDATA_IGPU	R35	0.4	DDCDATA

<15>	CRT_R_DGPU	R22	0.4	CRT_R
<15>	CRT_G_DGPU	R25	0.4	CRT_G
<15>	CRT_B_DGPU	R28	0.4	CRT_B
<15,16>	HSYNC_COM_DGPU	R20	0.4	HSYNC_COM
<15,16>	VSYNC_COM_DGPU	R18	0.4	VSYNC_COM
<15>	DDCCLK_DGPU	R31	0.4	DDCCLK
<15>	DDCDDATA_DGPU	R30	0.4	DDCDDATA



PU for internal CLK input
Unstuff for external XTAL(12MHz)

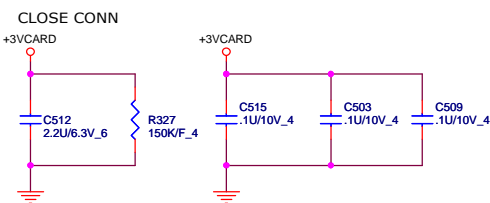


5 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/XD Cards

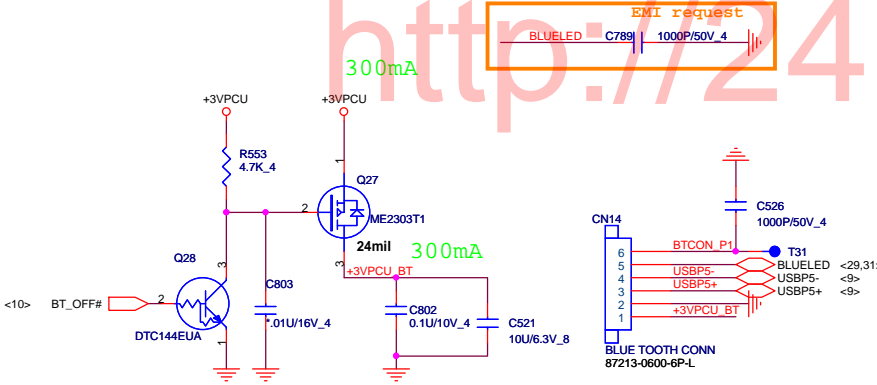
Note:

SD/MMC	MS	XD
SP0		XD_CD#
SP1	SD_WP	
SP2	SD_CD#	
SP3	SD_CD#	XD D4
SP4	SD_DAT1	XD D5
SP5	MS_BS	XD D3
SP6	MS_D1	XD D2
SP7	SD_DAT0	XD D6
SP8	SD_DAT7	XD D2
SP9	MS_INS#	
SP10	SD_DAT6	XD D7
SP11	SD_CLK	MS_SCLK
SP12	SD_DAT5	XD D0
SP13	SD_DAT4	XD WP#
SP14	SD_DAT3	XD R/B#
SP15	SD_DAT2	XD WE#
SP16	SD_DAT2	XD RE#
SP17		XD ALE
SP18		XD CE#
SP19		XD CLE

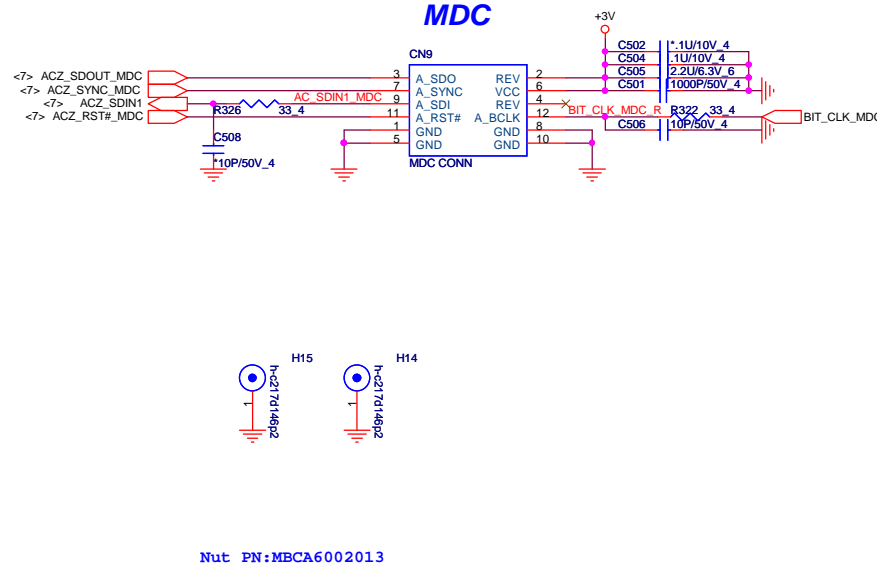


PROJECT :AX1
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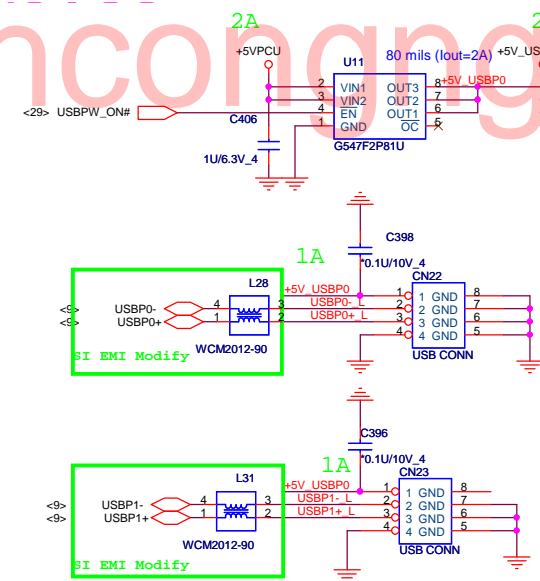
BLUETOOTH



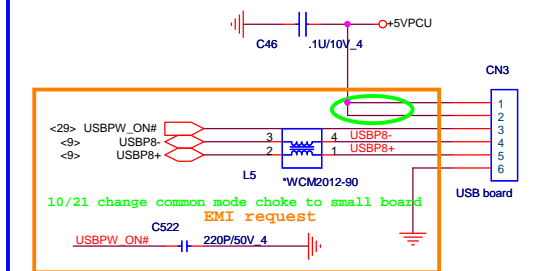
Modem CONN



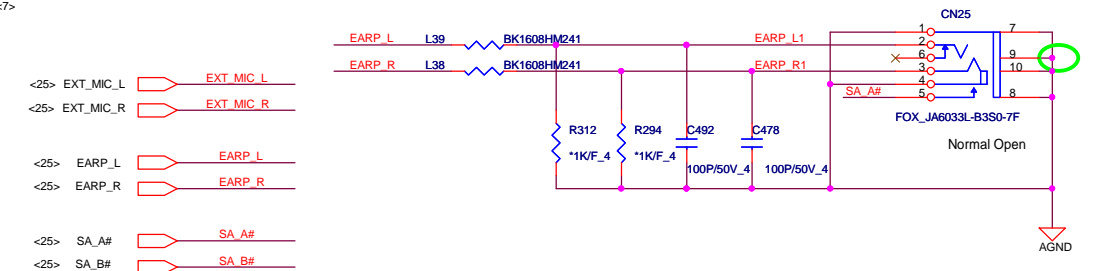
LEFT SIDE USBX1



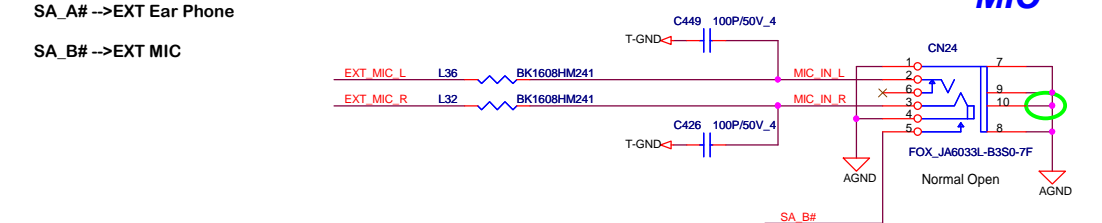
Right SIDE USBX1



Line out



MIC

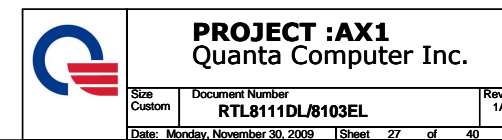
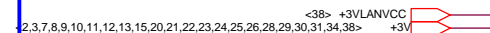
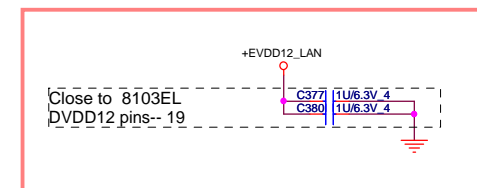


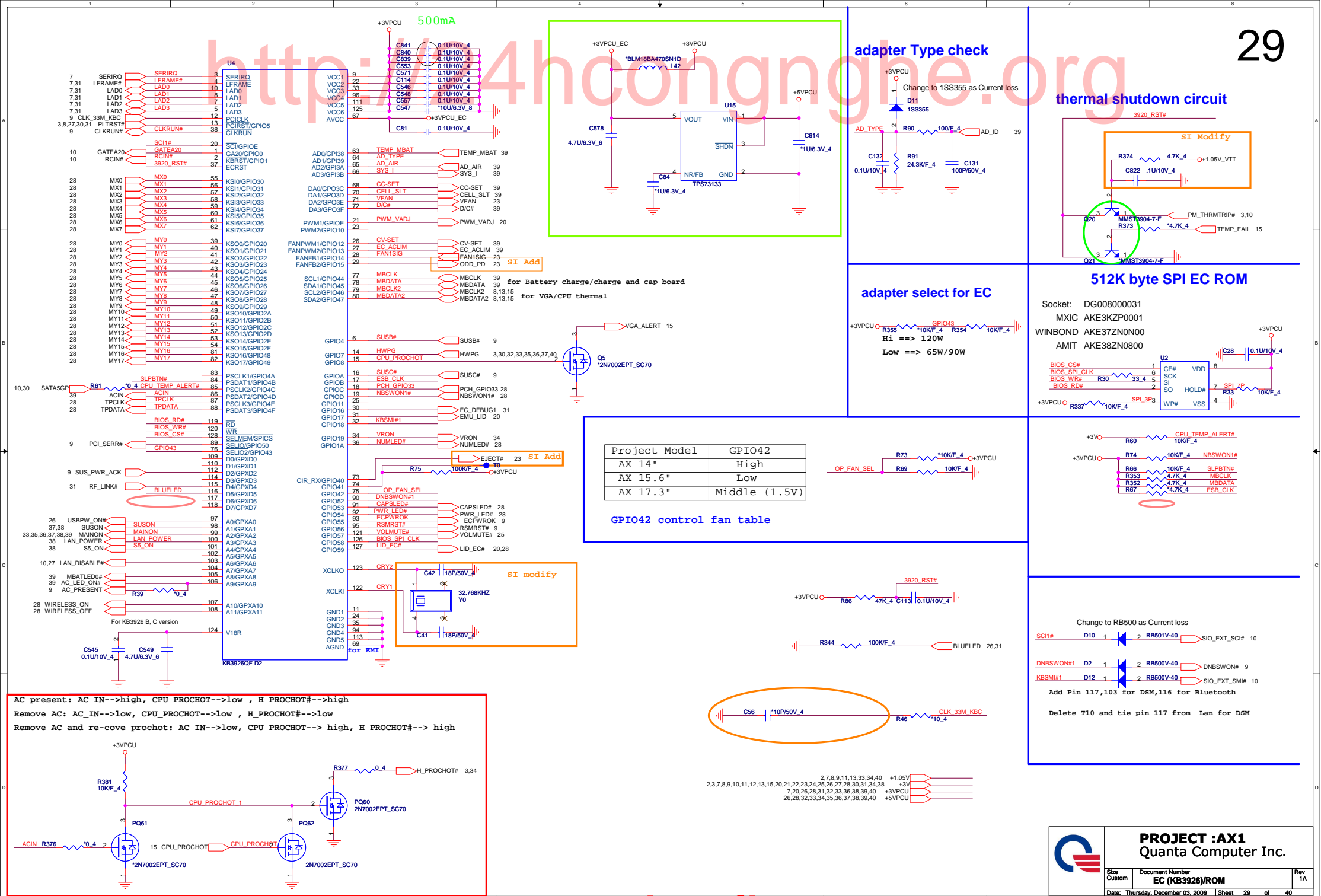
SA_A# -->EXT Ear Phone
SA_B# -->EXT MIC

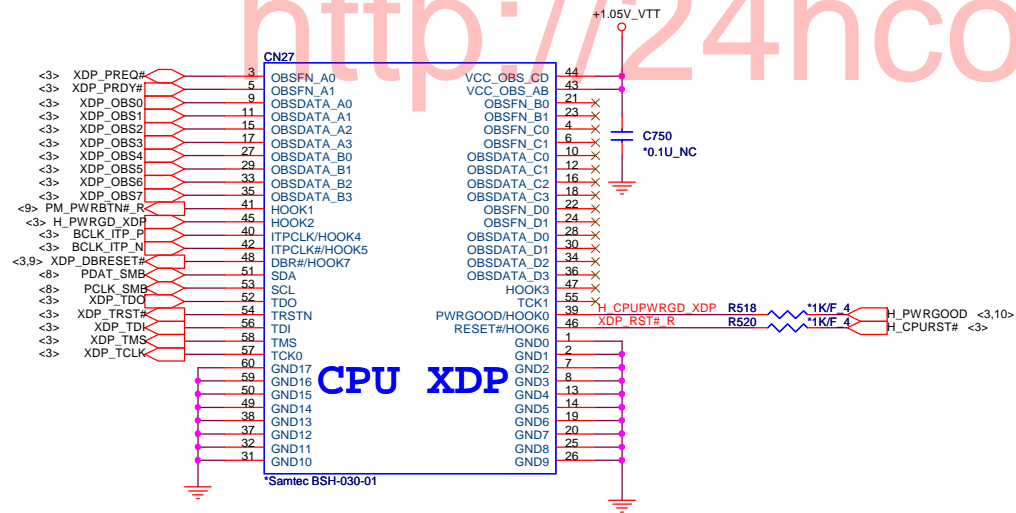


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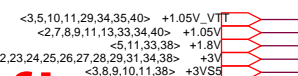
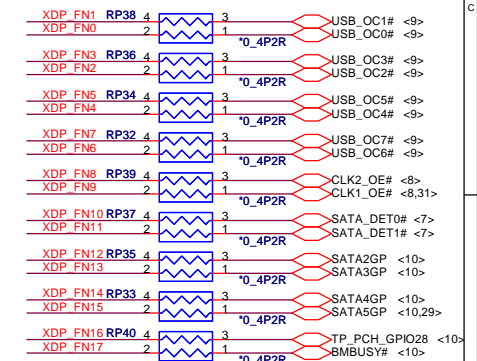
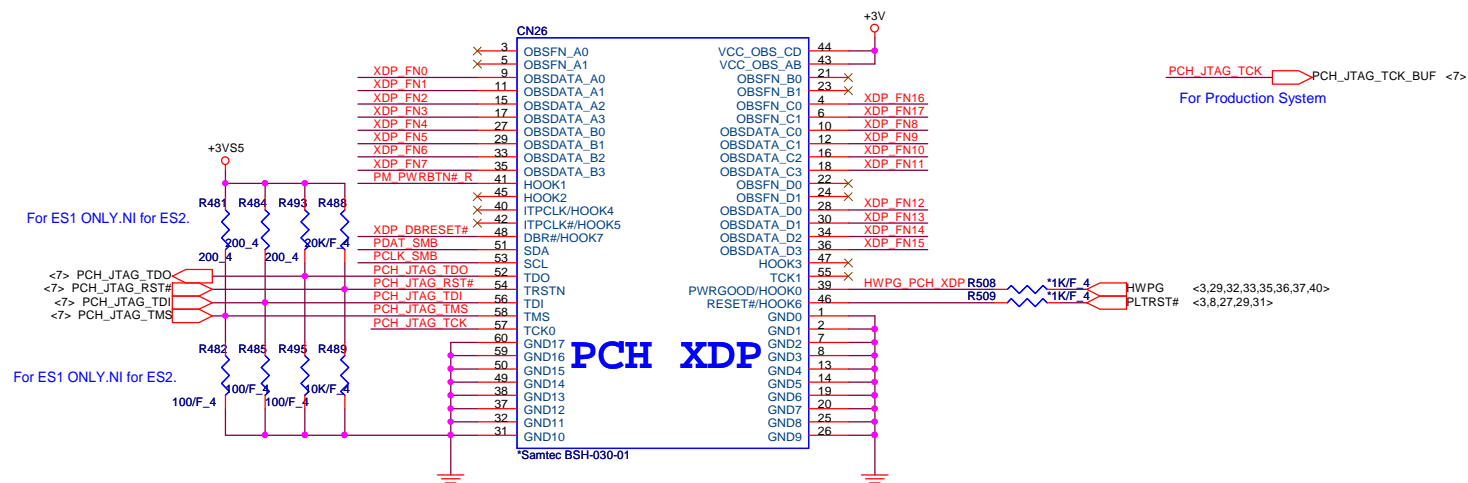
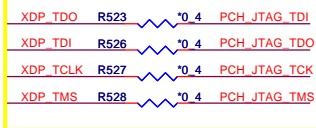
Size	Document Number	Rev
Custom	USB/BT/Modem/Audio JackK	1A
Date:	Monday, November 30, 2009	Sheet 26 of 40





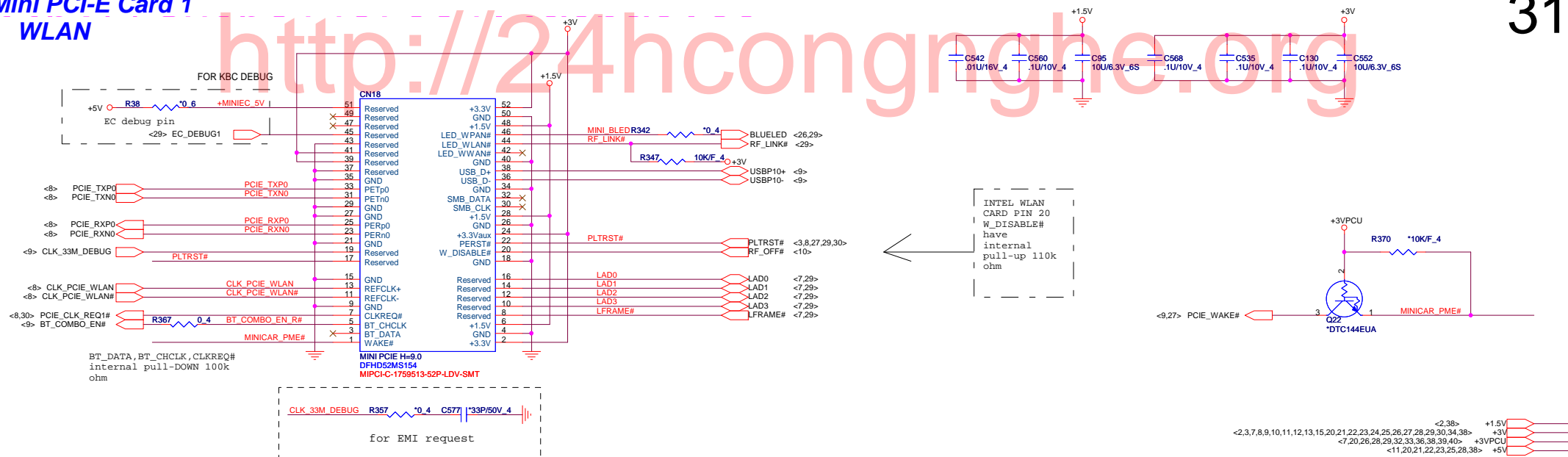


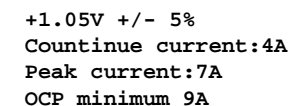
Reserve for BSDL



Mini PCI-E Card 1 WLAN

31





$$V_o = 0.75(R_1 + R_2) / R_2$$

$$V_o = 0.75(R_1 + R_2) / R_2$$

+1.8V Volt +/- 5%
Countinue current:1A
Peak current:2A
OCP minimum 3A

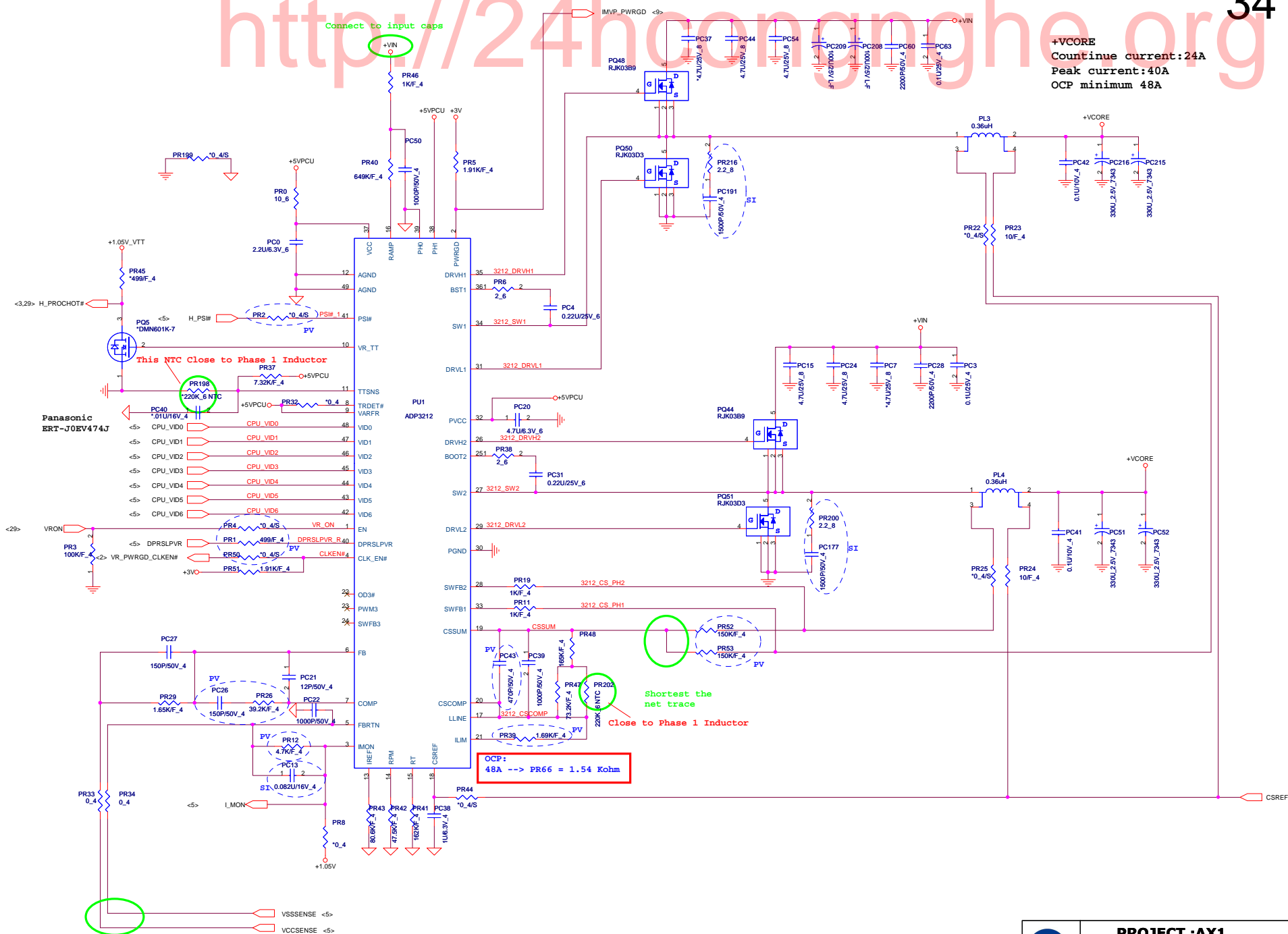


Size Custom	Document Number +1.05V/+1.8V (RT8204C)
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	Re
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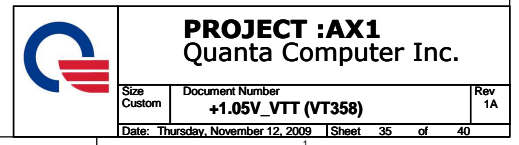
Date: Thursday, November 12, 2009	Sheet 33 of 4
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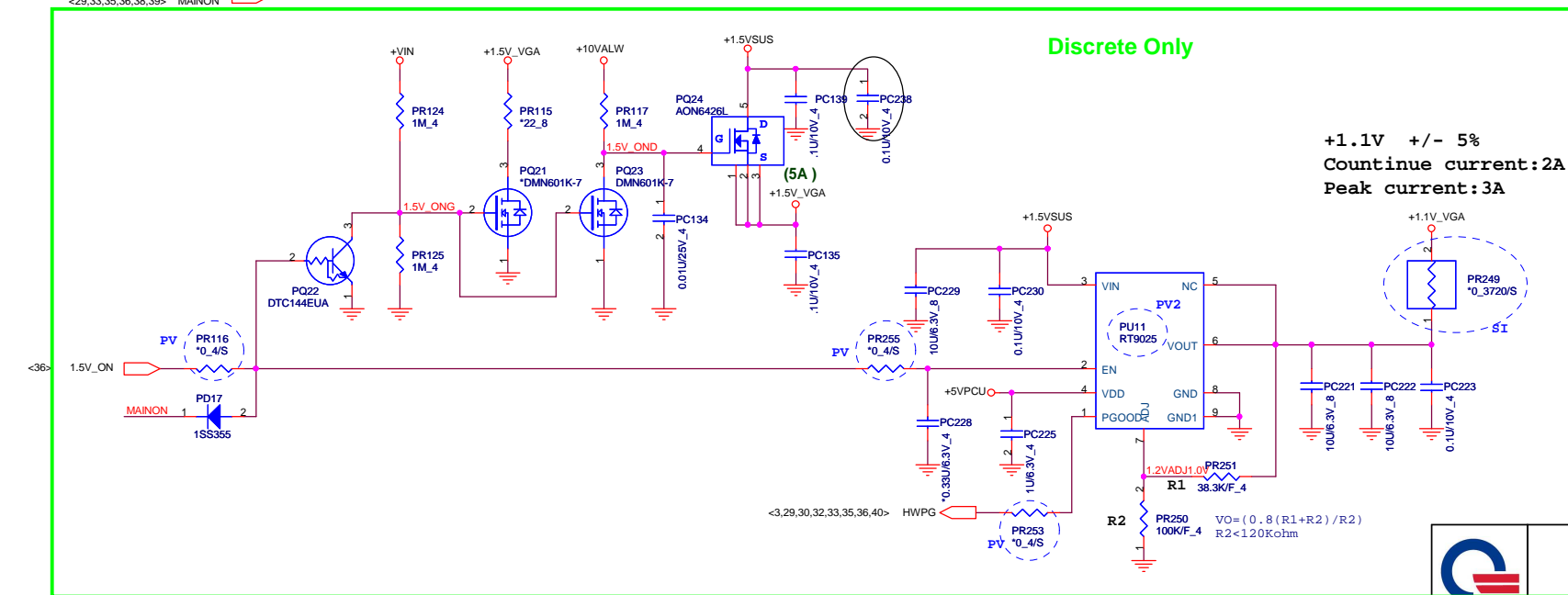
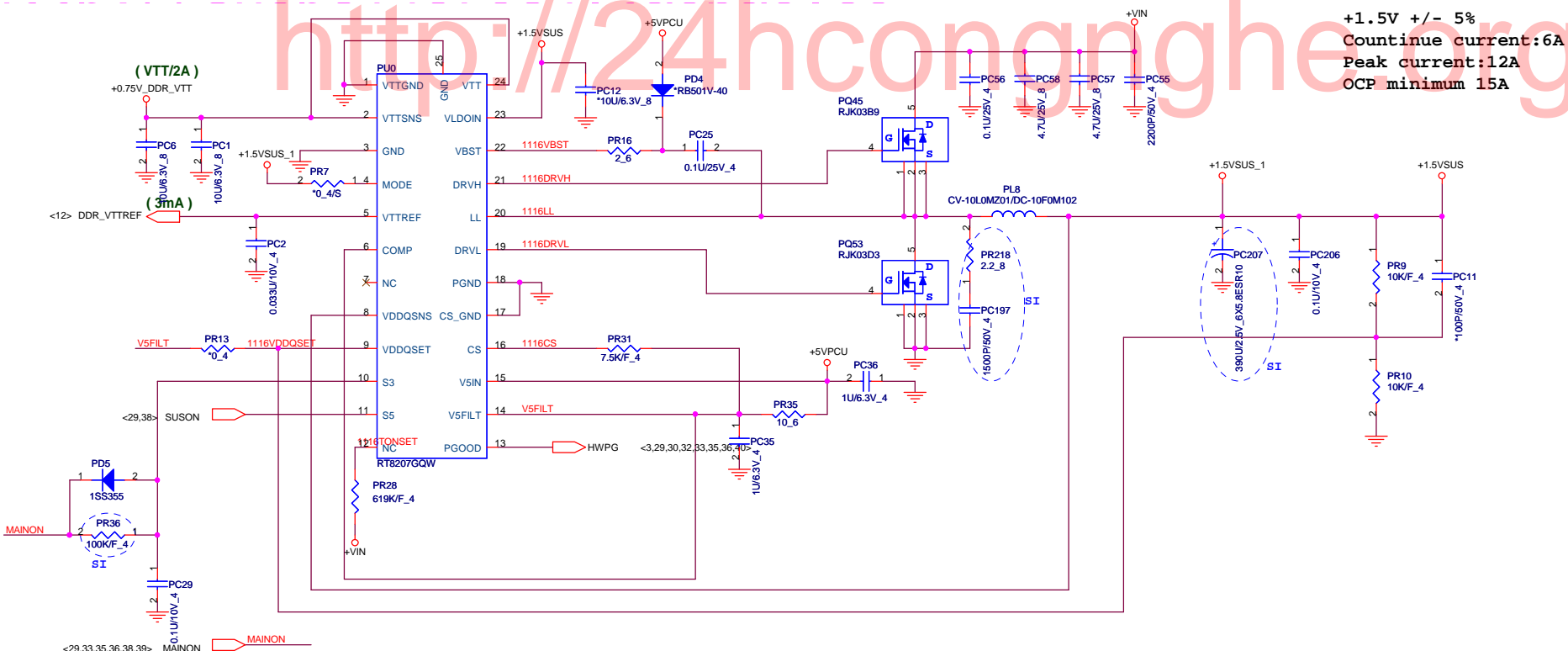
<http://24hcongnghe.org>



PROJECT :AX1
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Size Custom	Document Number CPU Core (ADP3212)	Rev 1A
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Size Custom	Document Number DDR3 (RT8207)	Rev 1A
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